WHAT IS CLAIMED IS:

1. An integrated packet bit error rate tester comprising:

a packet transmit circuit including a first memory for storing transmit packet data and connectable to a channel under test;

a packet receive circuit including a second memory for storing received packet compare data and connectable to the channel under test; and

an interface for programming the packet transmit and packet receive circuits,

wherein the packet transmit circuit can generate an arbitrary packet pattern in response to commands from the interface, and

wherein the packet receive circuit can determine a bit error rate of the channel under test.

2. The integrated packet bit error rate tester of claim **1**, wherein the packet transmit circuit includes a first pseudo-random number generator for generating the arbitrary packet pattern.

3. The integrated packet bit error rate tester of claim **2**, wherein the packet receive circuit includes a second pseudo-random number generator for generating the same arbitrary packet pattern that is generated by the first pseudo-random number generator.

4. The integrated packet bit error rate tester of claim **1**, wherein the packet transmit circuit includes a byte counter for counting the number of bytes transmitted during bit error rate testing.

5. The integrated packet bit error rate tester of claim **1**, wherein the packet transmit circuit includes a packet counter for counting the number of packets transmitted during bit error rate testing.

6. The integrated packet bit error rate tester of claim **1**, wherein the packet receive circuit includes a bit error counter for counting a number of bit errors detected during bit error rate testing.

7. The integrated packet bit error rate tester of claim **1**, wherein the packet receive circuit includes a byte error counter for counting a number of bytes with at least one bit in error detected during bit error rate testing.

8. The integrated packet bit error rate tester of claim **1**, wherein the packet receive circuit includes a packet error counter for counting a number of packets with at least one byte in error detected during bit error rate testing.

9. The integrated packet bit error rate tester of claim **1**, wherein the second memory captures the received packet data only after a pre-programmed pattern is detected.

10. The integrated packet bit error rate tester of claim **9**, wherein the pre-programmed pattern includes a fixed pattern.

11. The integrated packet bit error rate tester of claim **9**, wherein the pre-programmed pattern includes a programmable pattern.

12. The integrated packet bit error rate tester of claim **9**, wherein the pre-programmed pattern includes a CRC pattern.

13. The integrated packet bit error rate tester of claim **1**, wherein the arbitrary packet pattern is received from an external RAM.

14. The integrated packet bit error rate tester of claim **1**, wherein the arbitrary packet pattern can be loaded into a Random Access Memory for bit error rate testing.

15. The integrated packet bit error rate tester of claim **1**, wherein the second memory captures the received packet data only after a pre-programmed pattern is lost.

16. The integrated packet bit error rate tester of claim **1**, wherein the second memory captures the received packet data only after an error is detected.

17. The integrated packet bit error rate tester of claim **1**, wherein the second memory captures the received packet data immediately.

18. The integrated packet bit error rate tester of claim **1**, further including a finite state machine for controlling the capture of the received data.

19. The integrated packet bit error rate tester of claim **1**, wherein the packet receive circuit includes a byte counter for counting a total number of bytes received.

20. The integrated packet bit error rate tester of claim **1**, wherein the packet receive circuit includes a packet counter for counting a total number of packets received.

21. The integrated packet bit error rate tester of claim **1**, wherein the packet transmit circuit includes a byte counter for counting a total number of bytes transmitted.

22. The integrated packet bit error rate tester of claim **1**, wherein the packet transmit circuit includes a packet counter for counting a total number of packets transmitted.

23. The integrated packet bit error rate tester of claim **1**, wherein the arbitrary packet pattern is a 10G SERDES packet.

24. An integrated packet bit error rate tester comprising:

a packet transmit circuit including a first memory for storing transmit packet data and connectable to a channel under test;

a packet receive circuit including a second memory for capturing received packet compare data from the channel under test; and

an interface for programming the packet transmit and packet receive circuits,

wherein the packet transmit circuit can generate an arbitrary SERDES packet pattern in response to commands from the interface, and

wherein the packet receive circuit can determine a bit error rate of the channel under test based on the transmit packet data compared to the receive packet data.

25. The integrated packet bit error rate tester of claim **24**, wherein the packet receive circuit includes a byte counter for counting a total number of bytes received.

26. The integrated packet bit error rate tester of claim **24**, wherein the packet receive circuit includes a packet counter for counting a total number of packets received.

27. The integrated packet bit error rate tester of claim **24**, wherein the packet transmit circuit includes a byte counter for counting a total number of bytes transmitted.

28. The integrated packet bit error rate tester of claim **24**, wherein the packet transmit circuit includes a packet counter for counting a total number of packets transmitted.

29. The integrated packet bit error rate tester of claim **24**, wherein the packet transmit circuit includes a first pseudo-random number generator for generating the arbitrary SERDES packet pattern.

30. The integrated packet bit error rate tester of claim **29**, wherein the packet receive circuit includes a second pseudo-random number generator for generating the same arbitrary SERDES packet pattern that is generated by the first pseudo-random number generator.

31. The integrated packet bit error rate tester of claim **29**, wherein the second memory captures the received packet data only after a pre-programmed pattern is detected.

32. The integrated packet bit error rate tester of claim **31**, wherein the pre-programmed pattern includes a fixed pattern.

33. The integrated packet bit error rate tester of claim **31**, wherein the pre-programmed pattern includes a programmable pattern.

34. The integrated packet bit error rate tester of claim **31**, wherein the pre-programmed pattern includes a CRC pattern.

35. The integrated packet bit error rate tester of claim **24**, wherein the second memory captures the received packet data only after a pre-programmed pattern is lost.

36. The integrated packet bit error rate tester of claim **24**, wherein the second memory captures the received packet data only after an error is detected.

37. The integrated packet bit error rate tester of claim **24**, wherein the second memory captures the received packet data immediately.

38. An integrated packet bit error rate tester comprising:

a packet transmit circuit including a first memory for storing transmit packet data and connectable to a channel under test; and

a packet receive circuit including a second memory for capturing received packet data from the channel under test upon any one of (a) after a pre-programmed pattern is detected, (b) after a pre-programmed pattern is lost, (c) after an error is detected, and (d) immediately.

39. The integrated packet bit error rate tester of claim **38**, wherein the packet transmit circuit includes a first pseudo-random number generator for generating an arbitrary SERDES packet pattern for transmission over the channel under test.

40. The integrated packet bit error rate tester of claim **38**, wherein the packet receive circuit includes a second pseudo-random number generator for generating the same arbitrary SERDES packet pattern that is generated by the first pseudo-random number generator.

41. A method of testing bit error rate of a channel comprising:

generating a test packet including an arbitrary marker pattern;

transmitting the test packet over the channel;

capturing the test packet from the channel; and

determining the bit error rate of the channel based on the test packet.

42. The method of claim **41**, further including generating an arbitrary 10G SERDES packet pattern.

43. The method of claim **41**, further including generating the arbitrary 10G SERDES packet pattern using a first pseudo-random number generator.

44. The method of claim **41**, further including programming the arbitrary 10G SERDES packet pattern through a media independent input/output interface.

45. The method of claim **41**, further including generating the same arbitrary 10G SERDES packet pattern using a second pseudo-random number generator as the 10G SERDES packet pattern generated by the first pseudo-random number generator.

46. The method of claim **41**, further including counting a number of bytes received during the bit error rate testing.

47. The method of claim **41**, further including counting a number of packets received during the bit error rate testing.

48. The method of claim **41**, further including counting a number of bit errors detected during the bit error rate testing.

49. The method of claim **41**, further including counting a number of bytes with errors detected during the bit error rate testing.

50. The method of claim **41**, further including counting a number of packets with a byte in error detected during the bit error rate testing.

51. The method of claim **41**, further including determining a bit error rate of the channel under test.

52. The method of claim **41**, further including counting a number of packets transmitted over the channel.

53. The method of claim **41**, further including counting a number of number of bytes transmitted over the channel.